

FIG.1A

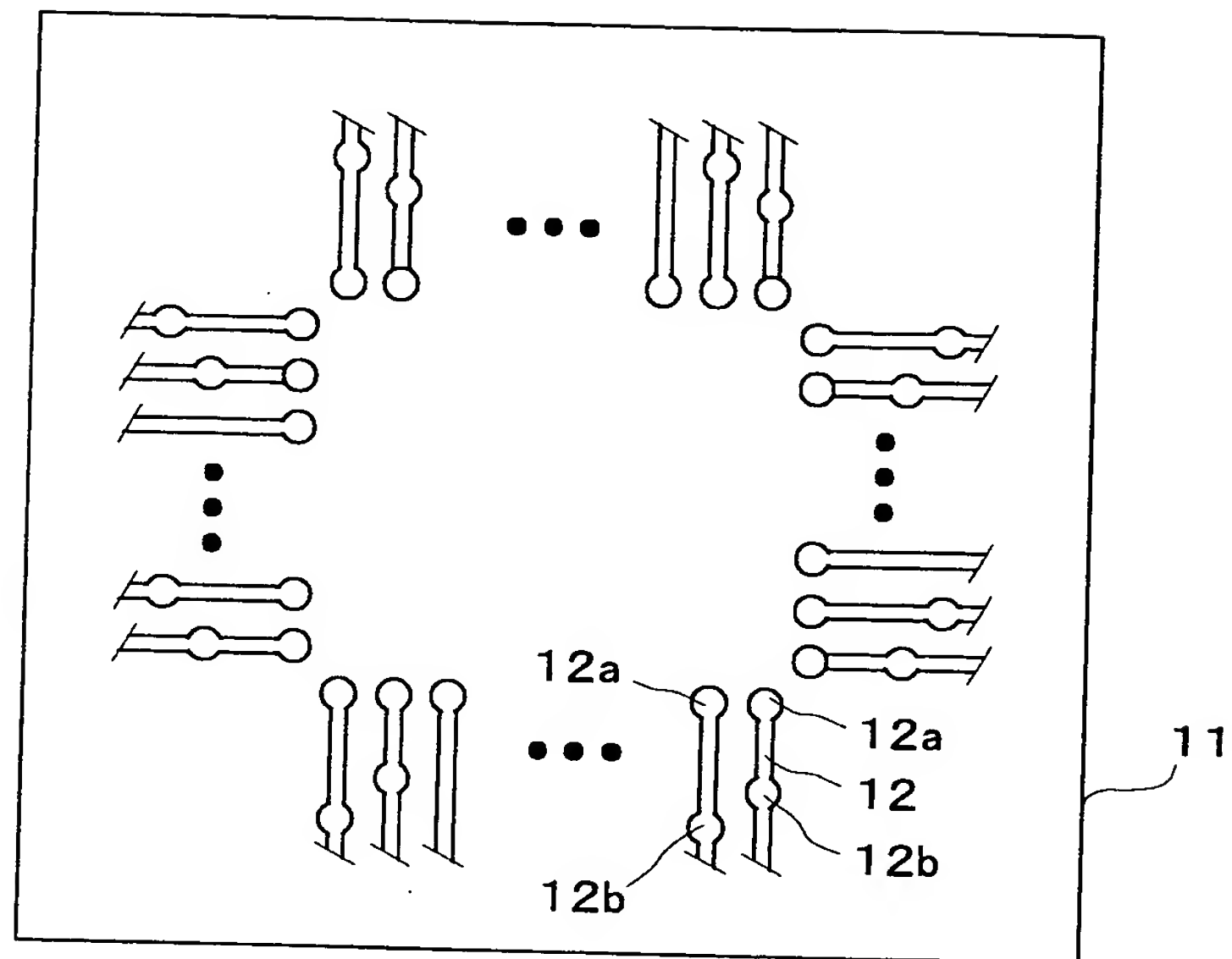


FIG.1B

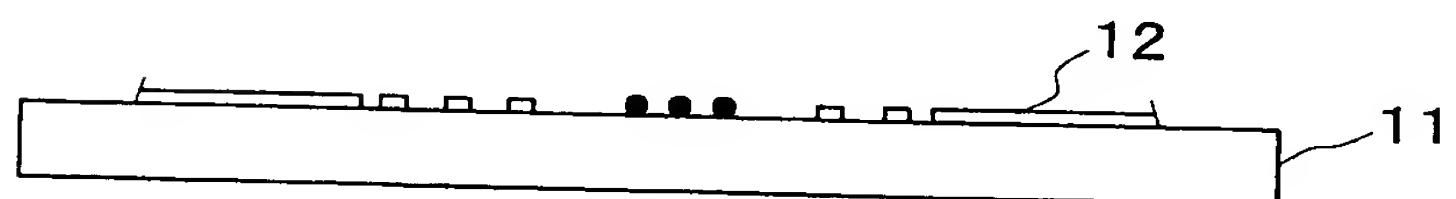


FIG.2A

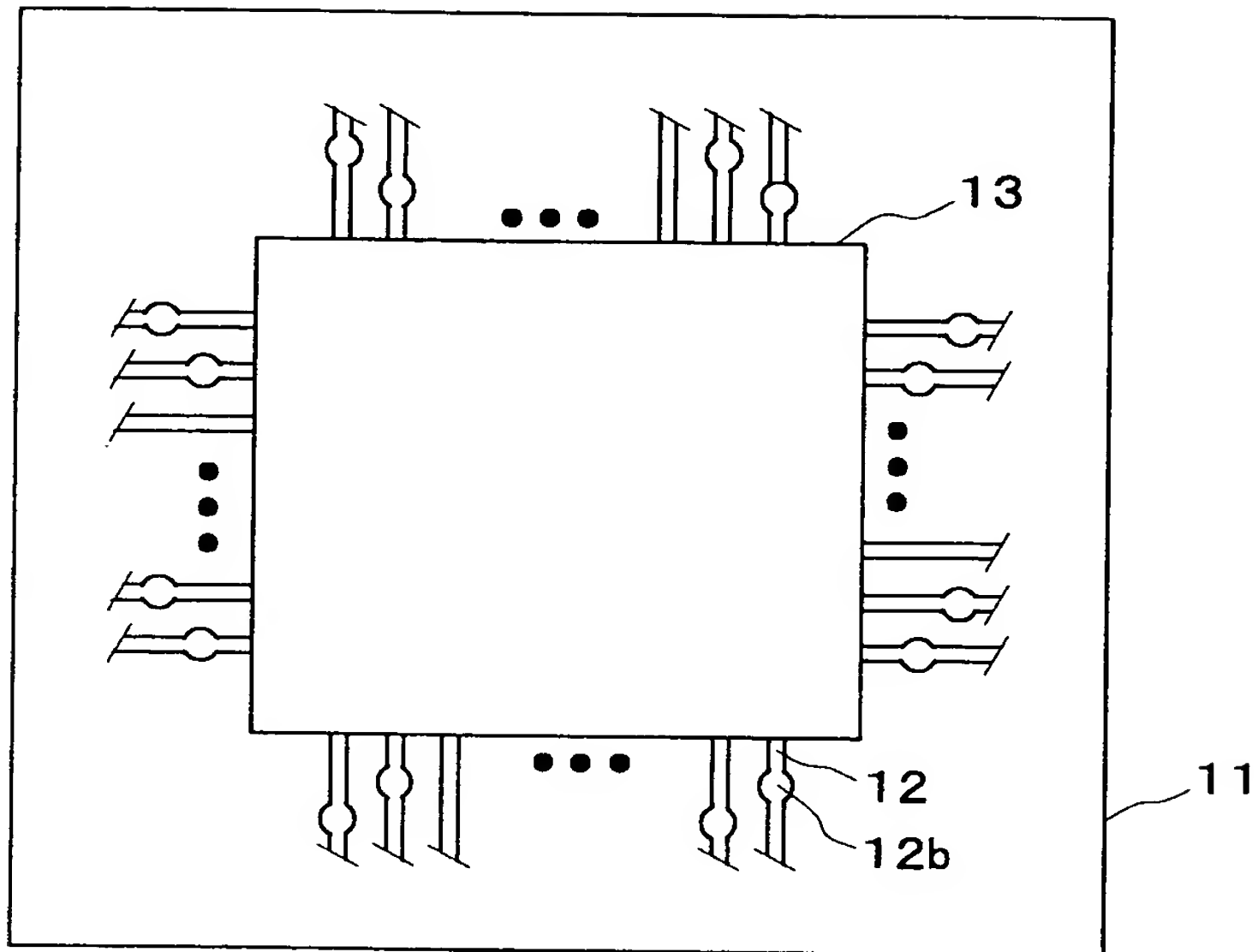


FIG.2B

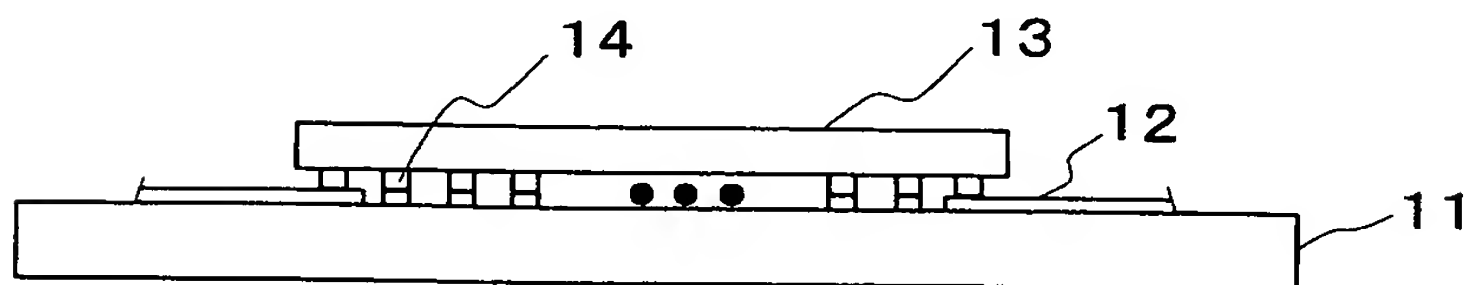


FIG.3A

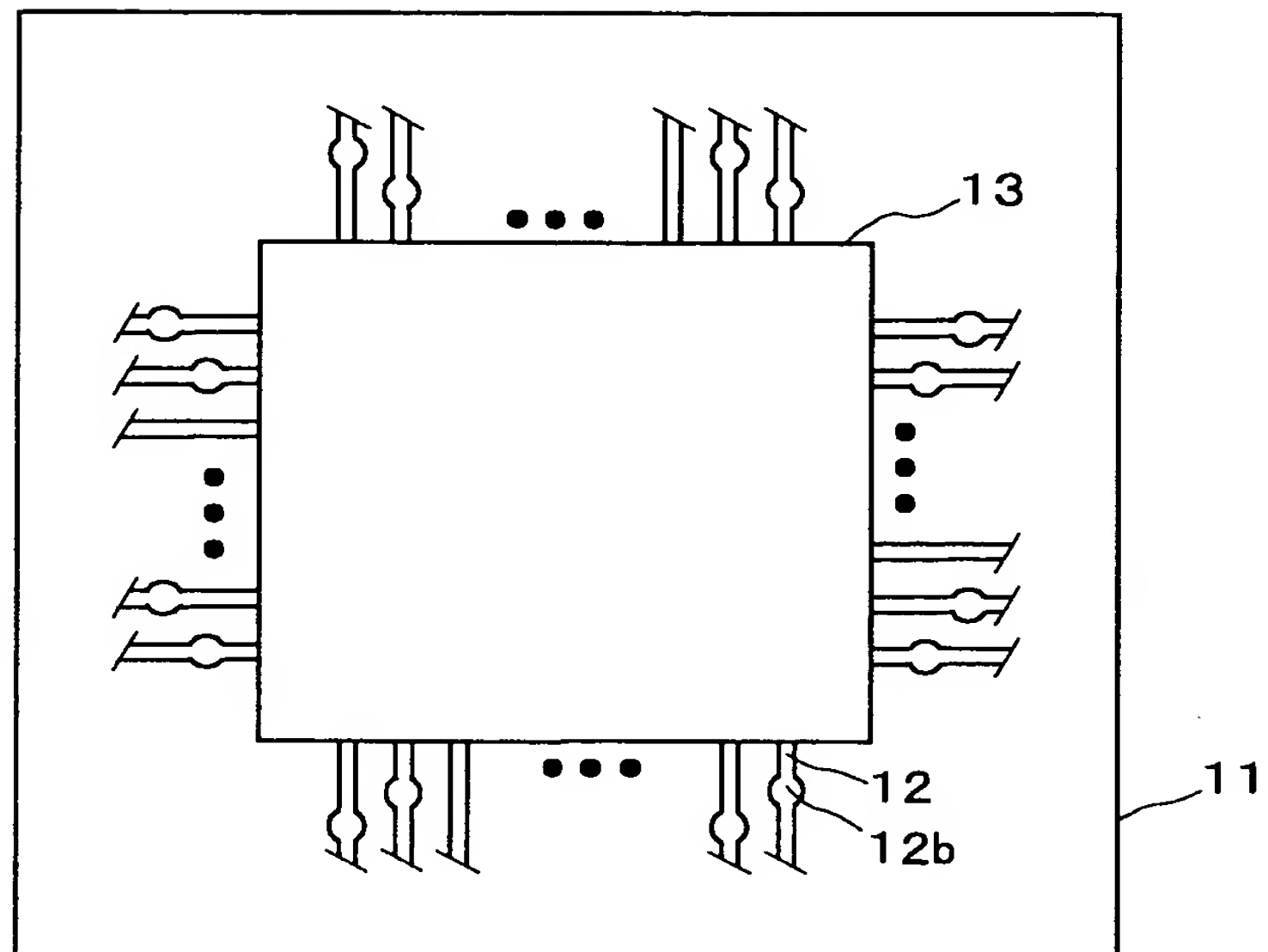


FIG.3B

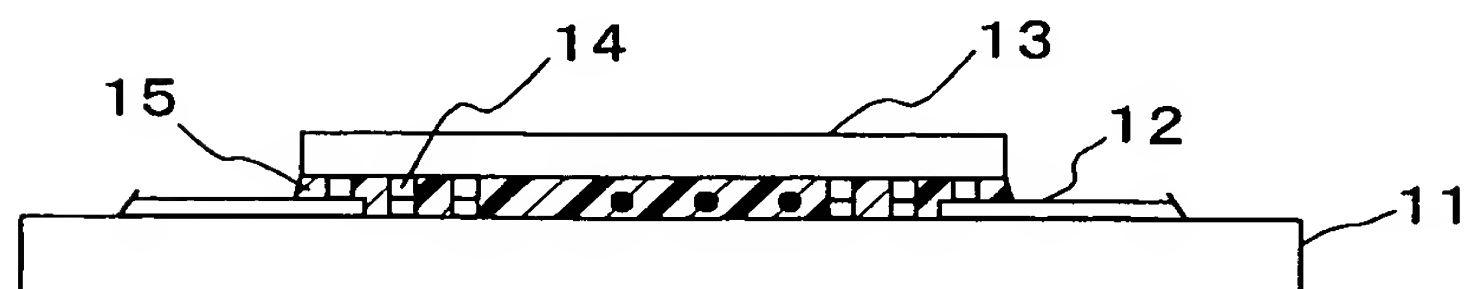


FIG.4A

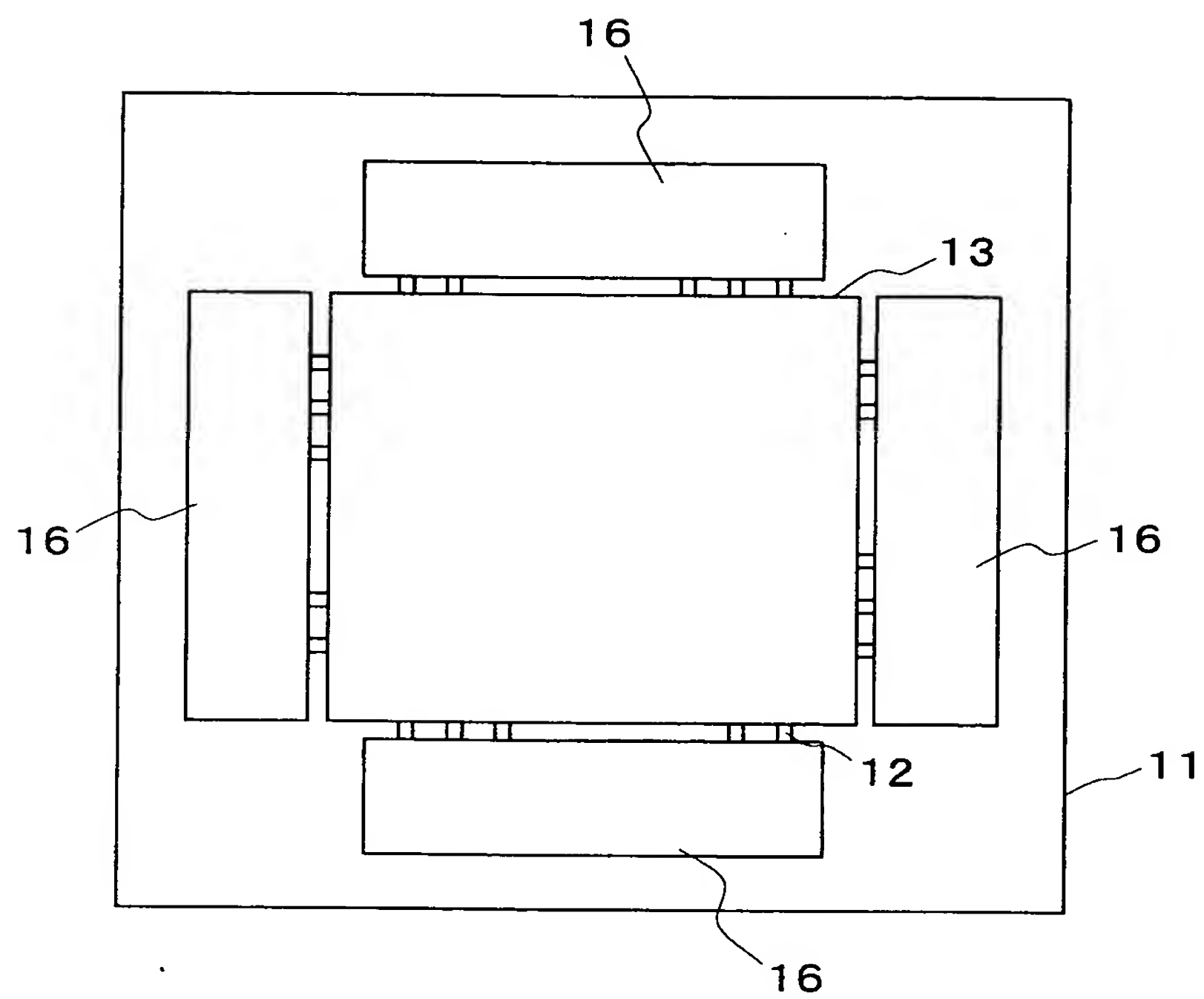
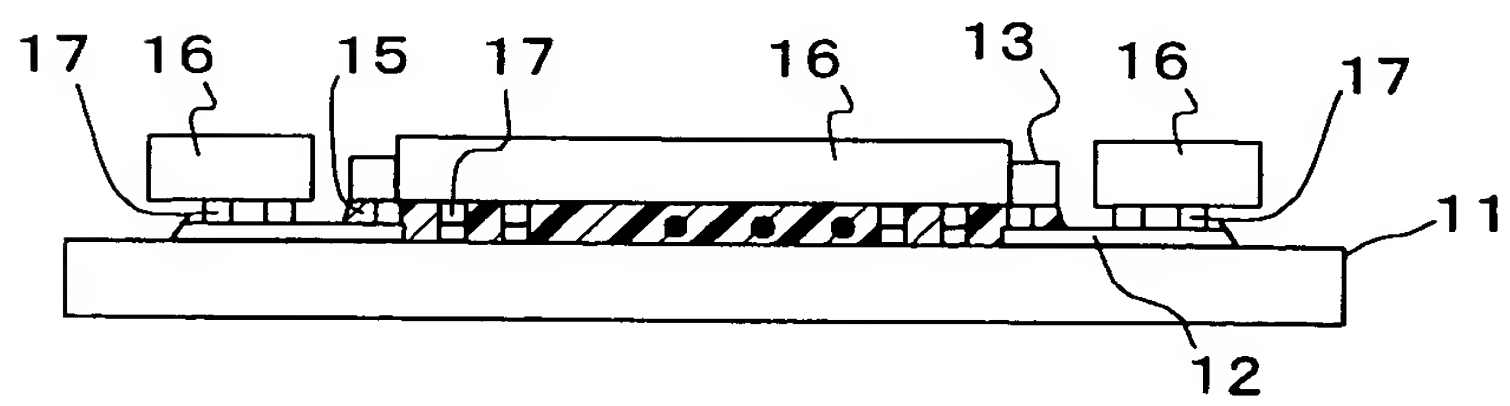


FIG.4B



A schematic diagram of a semiconductor device layout. The layout is enclosed in a rectangular frame labeled 11. In the center is a large square region labeled 12. Surrounding this central region are four rectangular regions: one at the top, one at the bottom, and two on the left and right sides. These four surrounding regions are collectively labeled 13. Each of these four regions is further divided into a grid of smaller rectangular sub-regions. The label 16 points to the top, bottom, and right-hand sub-regions, while the label 17 points to the left-hand sub-regions.

FIG.6

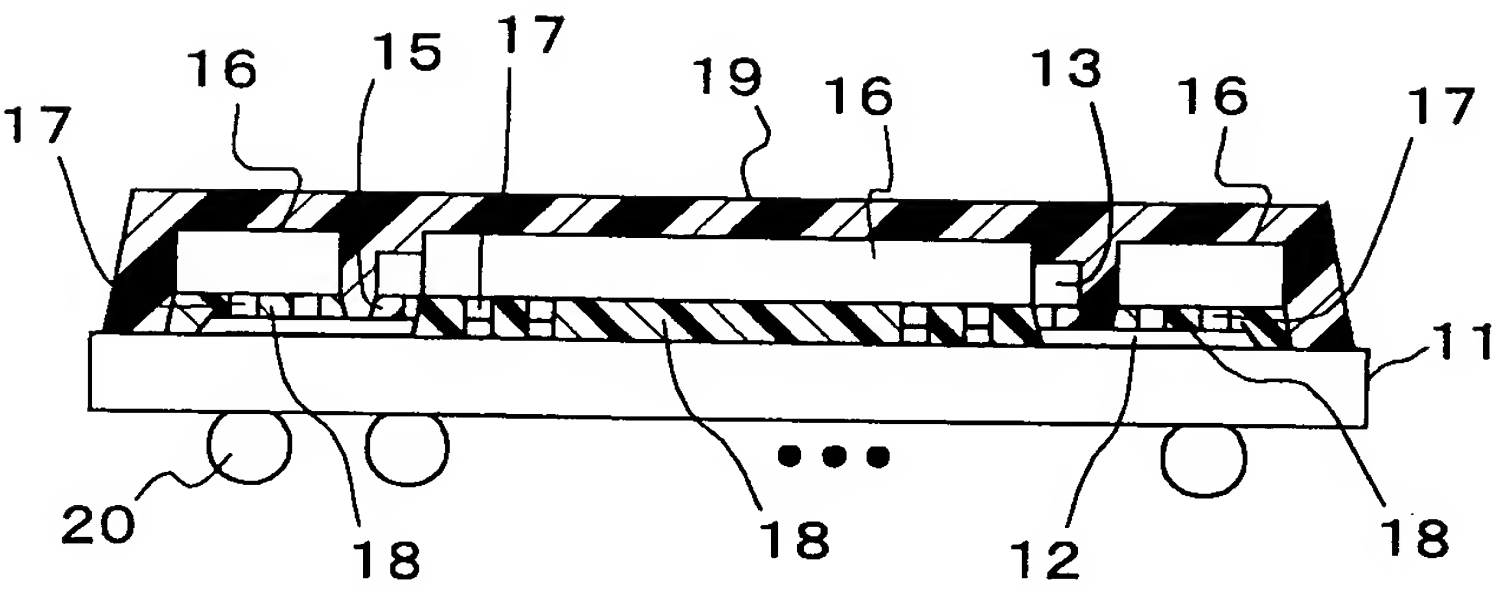


FIG. 7

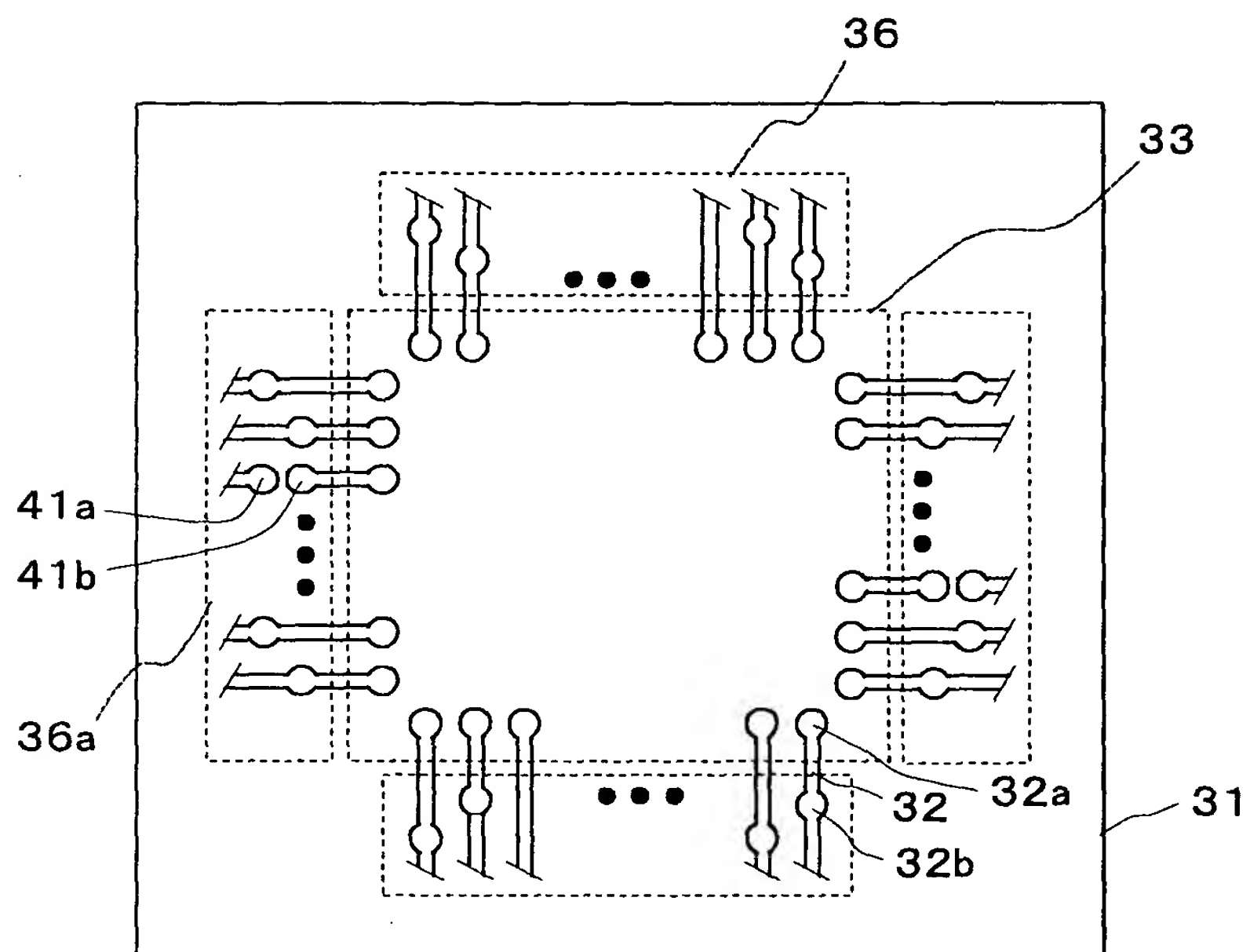
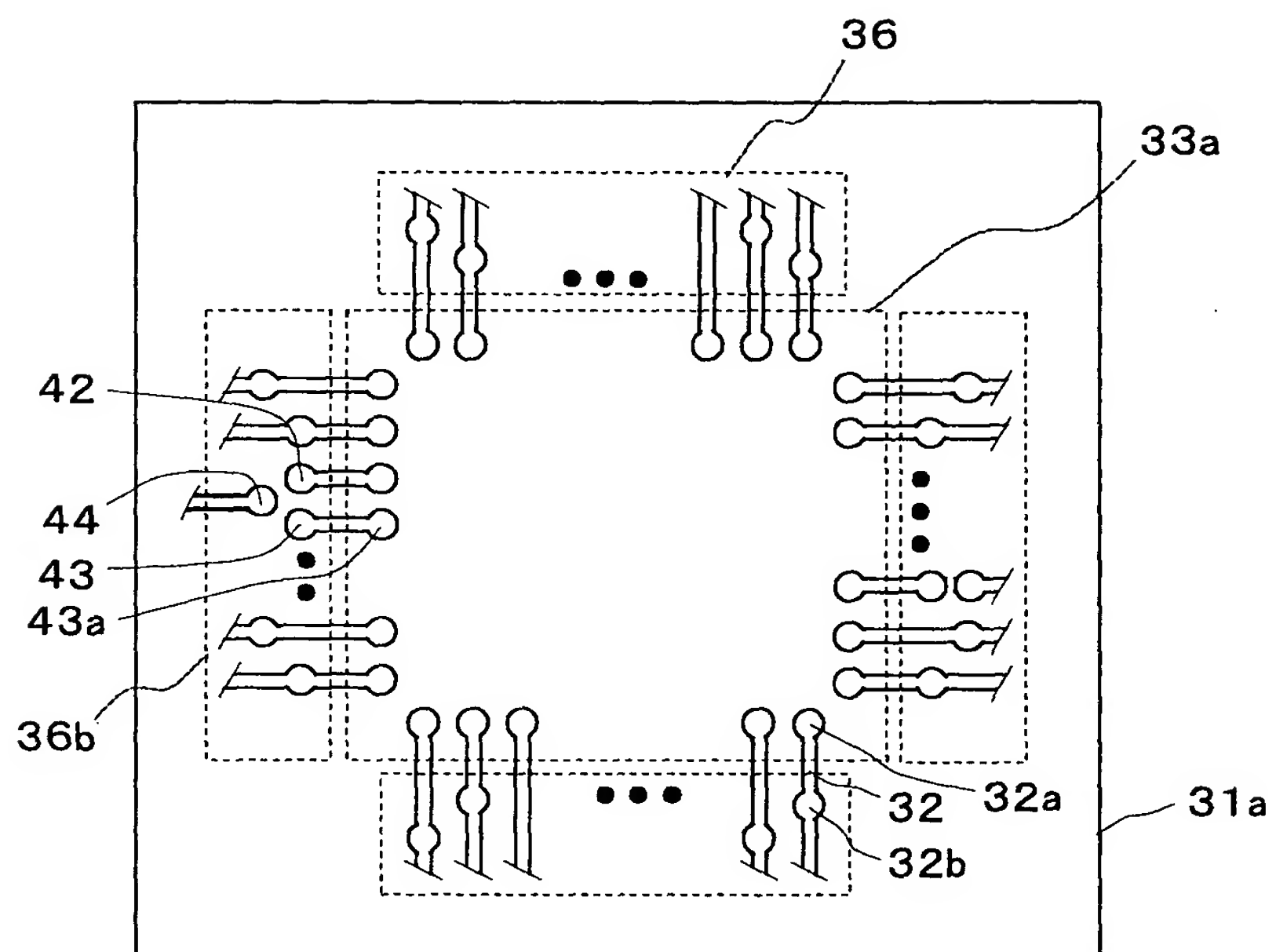
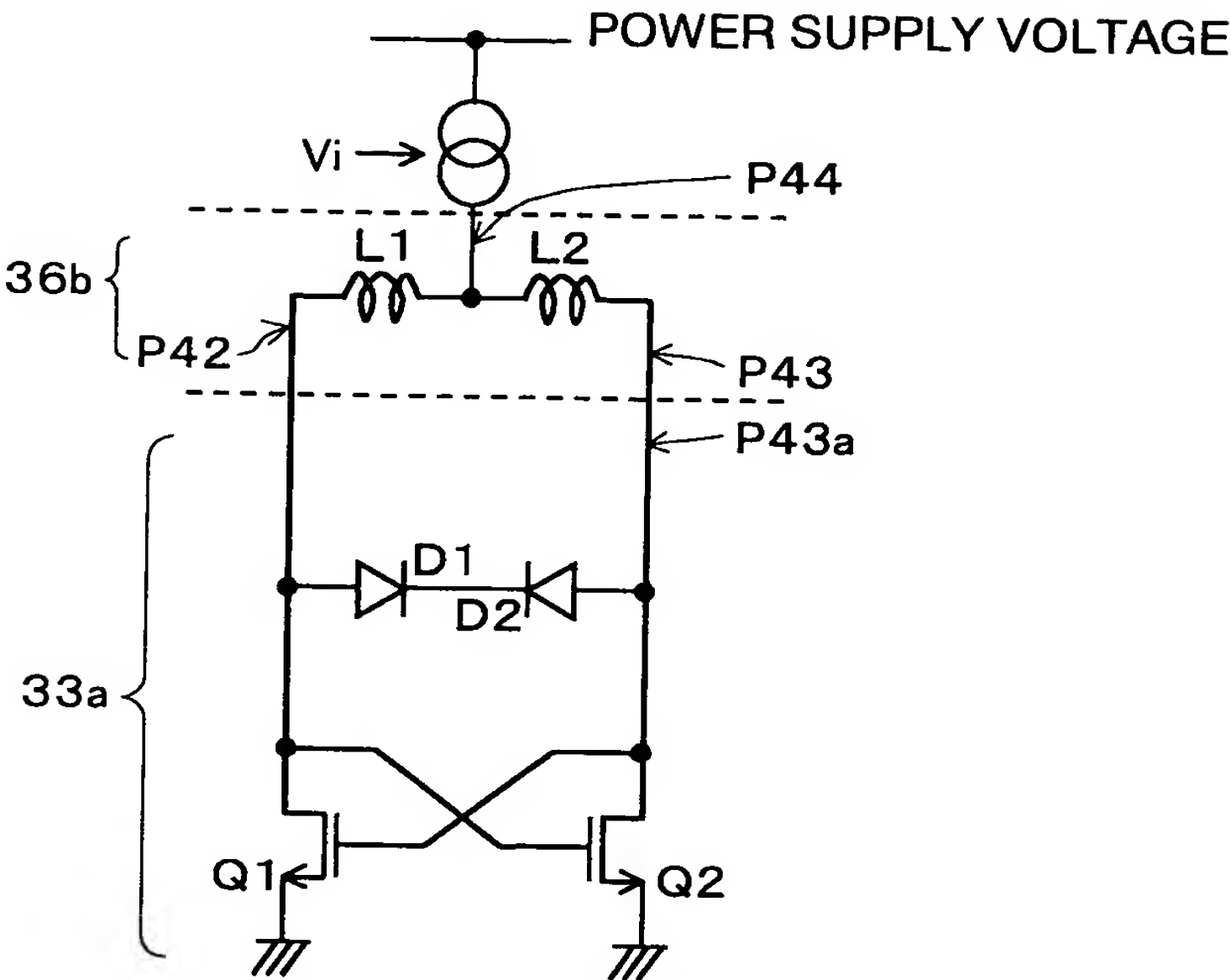


FIG.8





**FIG. 9A**



**FIG. 9B**

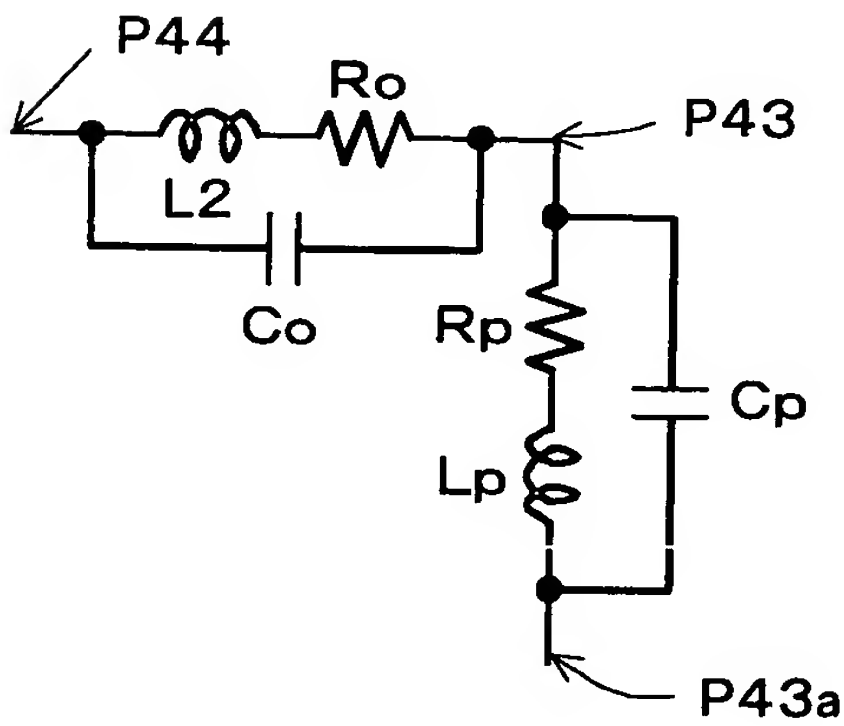


FIG.10

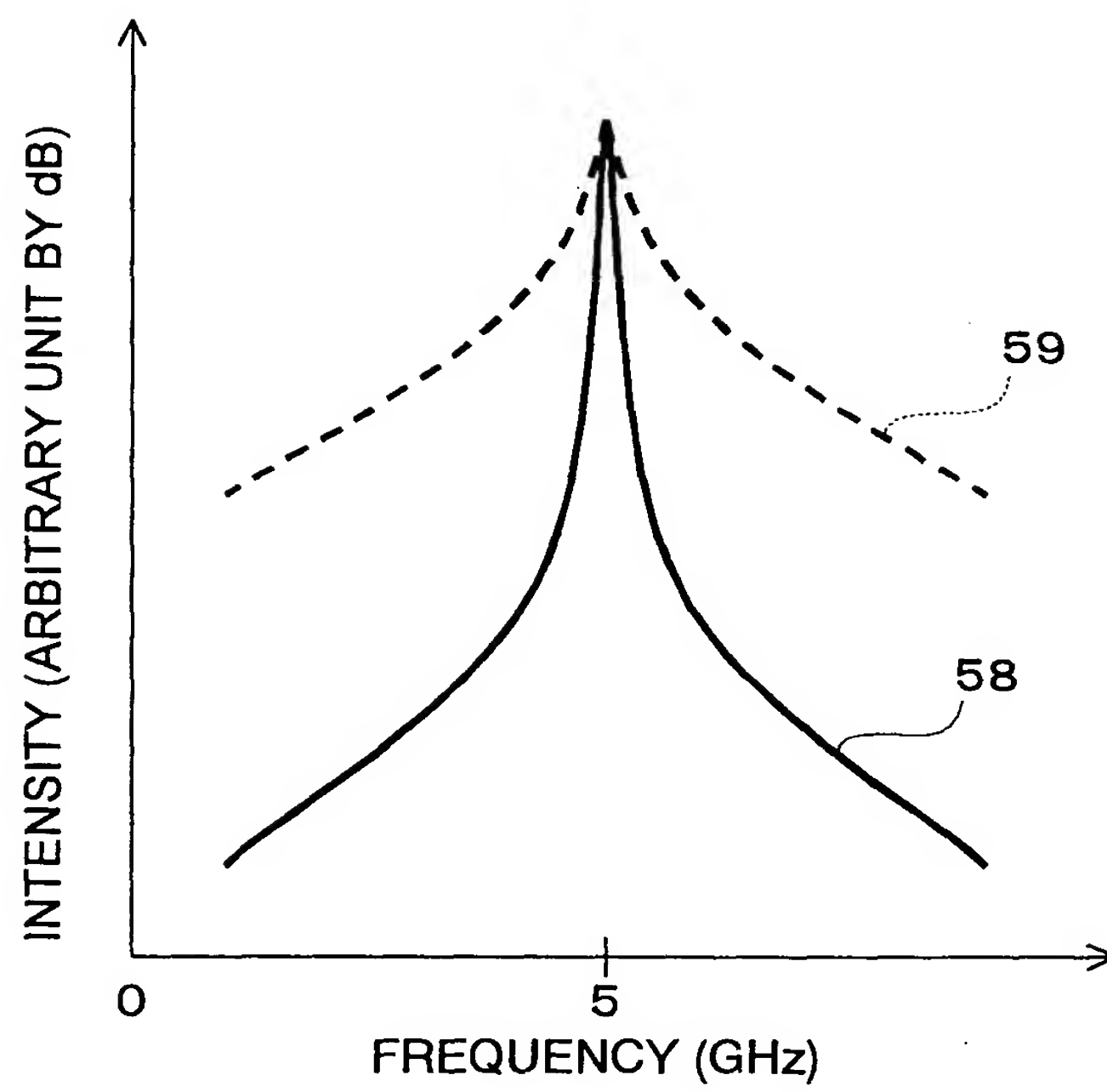


FIG. 11A

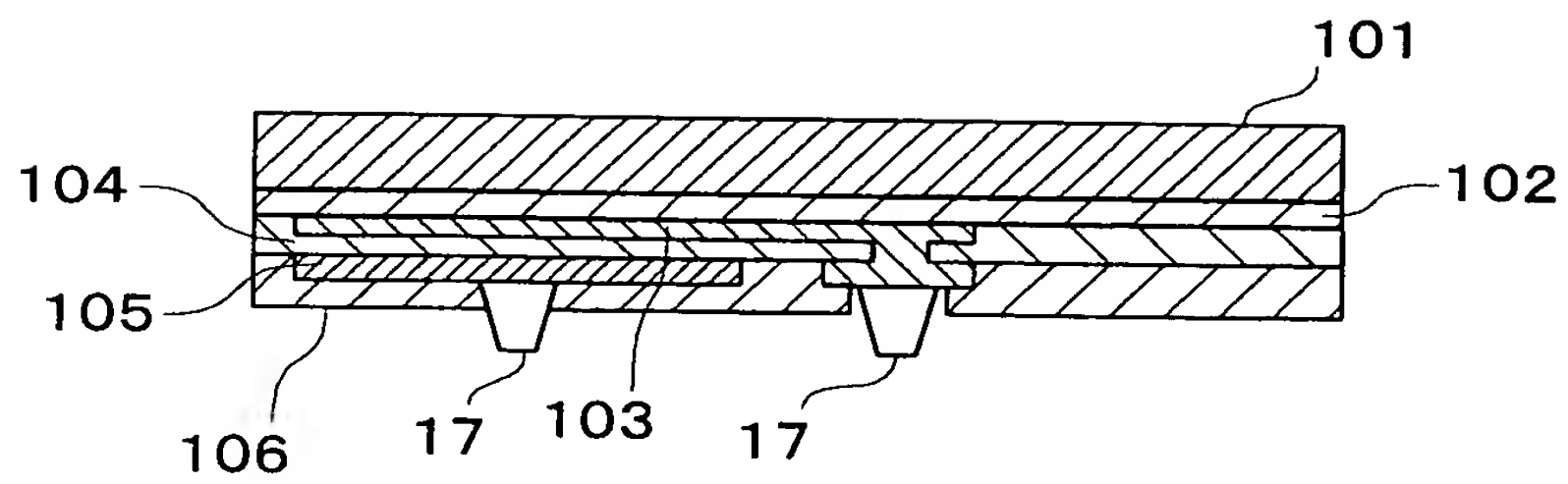


FIG. 11B

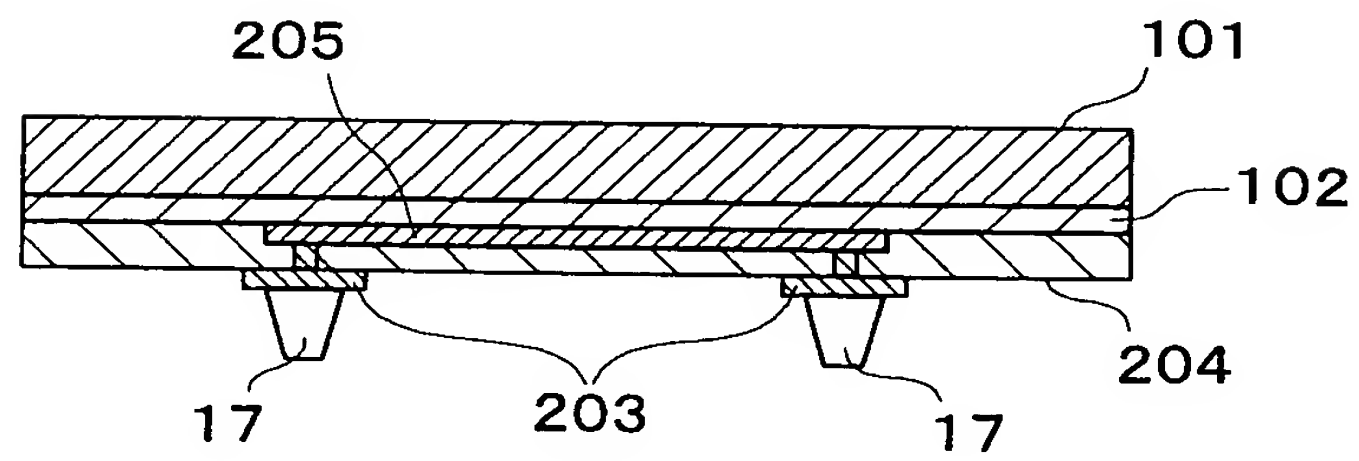


FIG. 11C

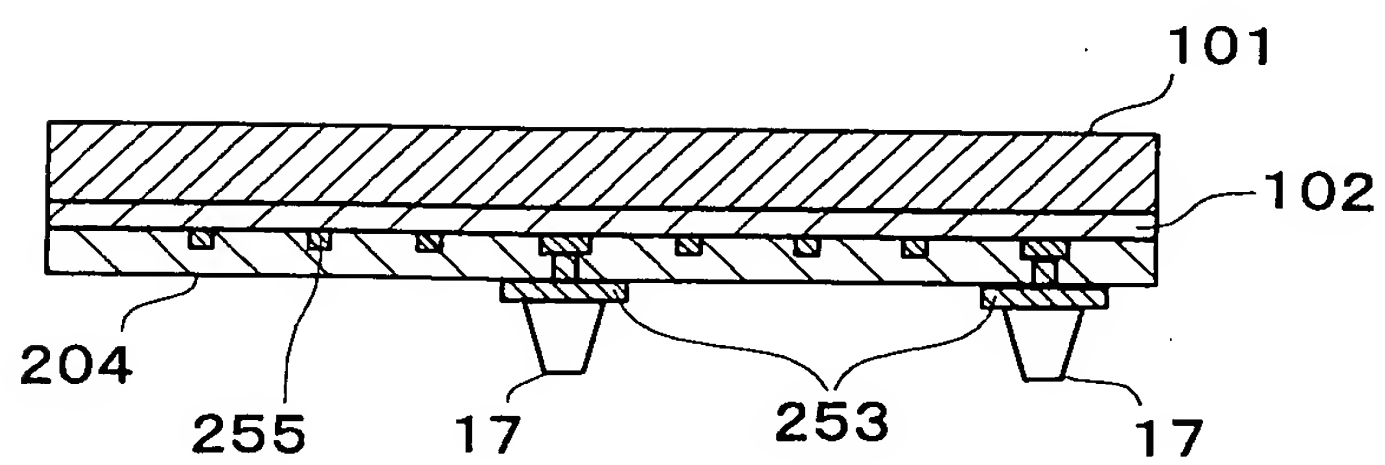


FIG.1 1 D

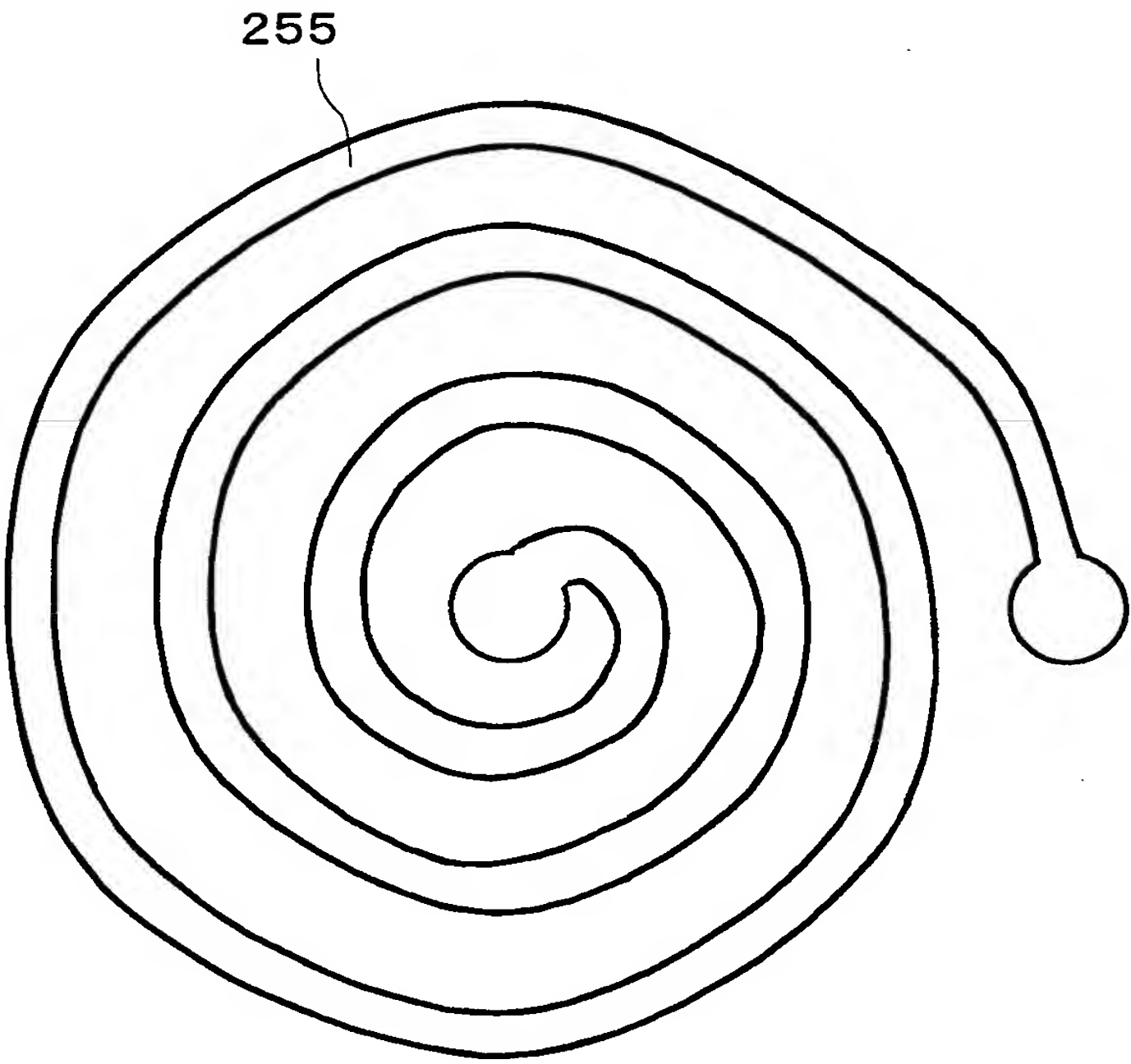


FIG. 12

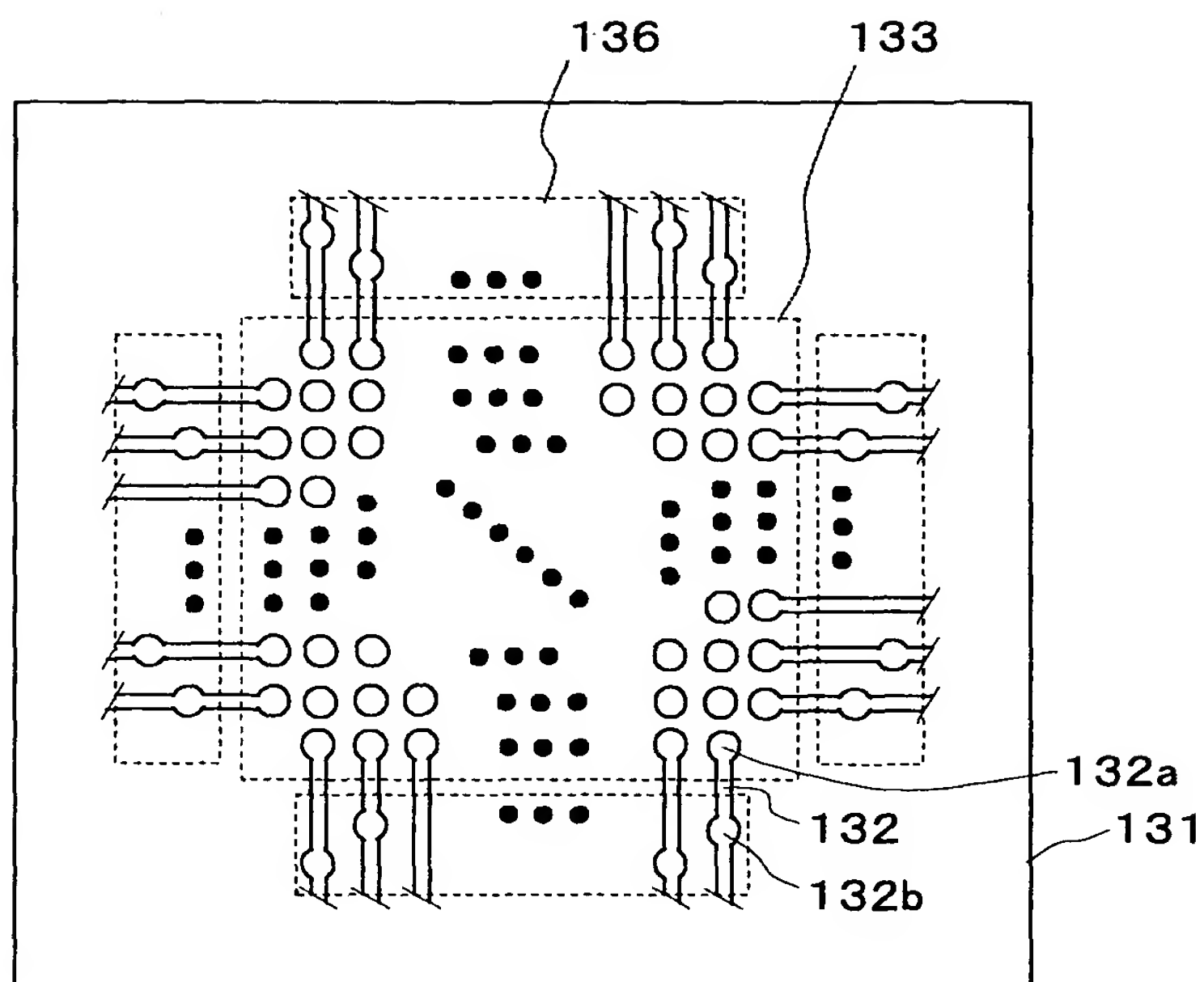


FIG.13A

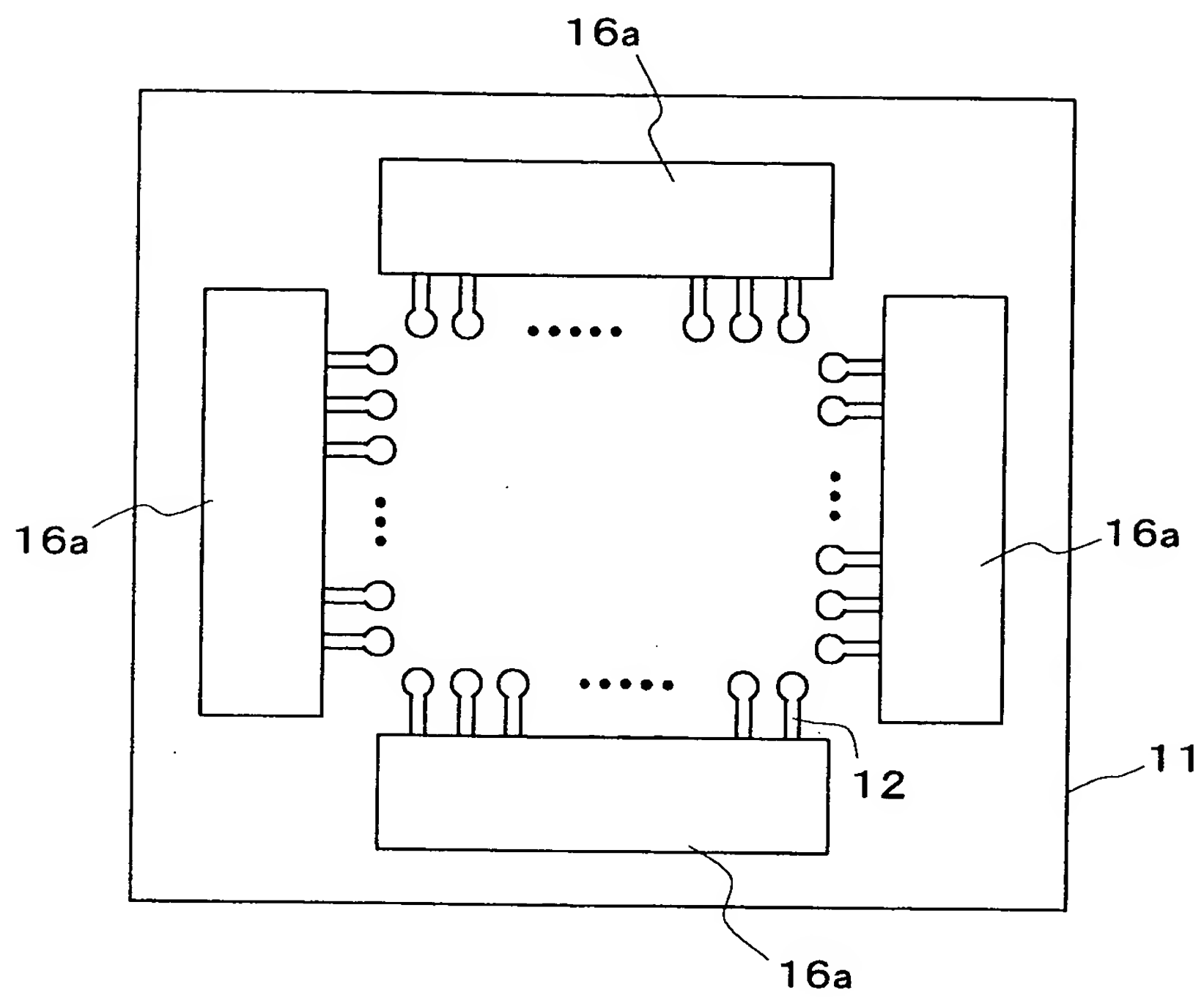


FIG.13B

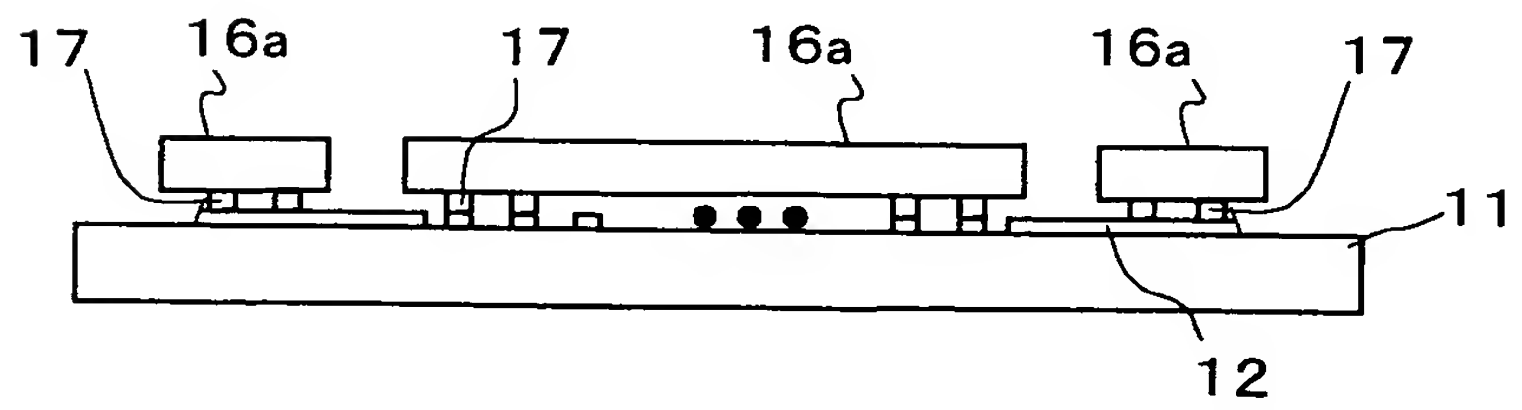


FIG.14A

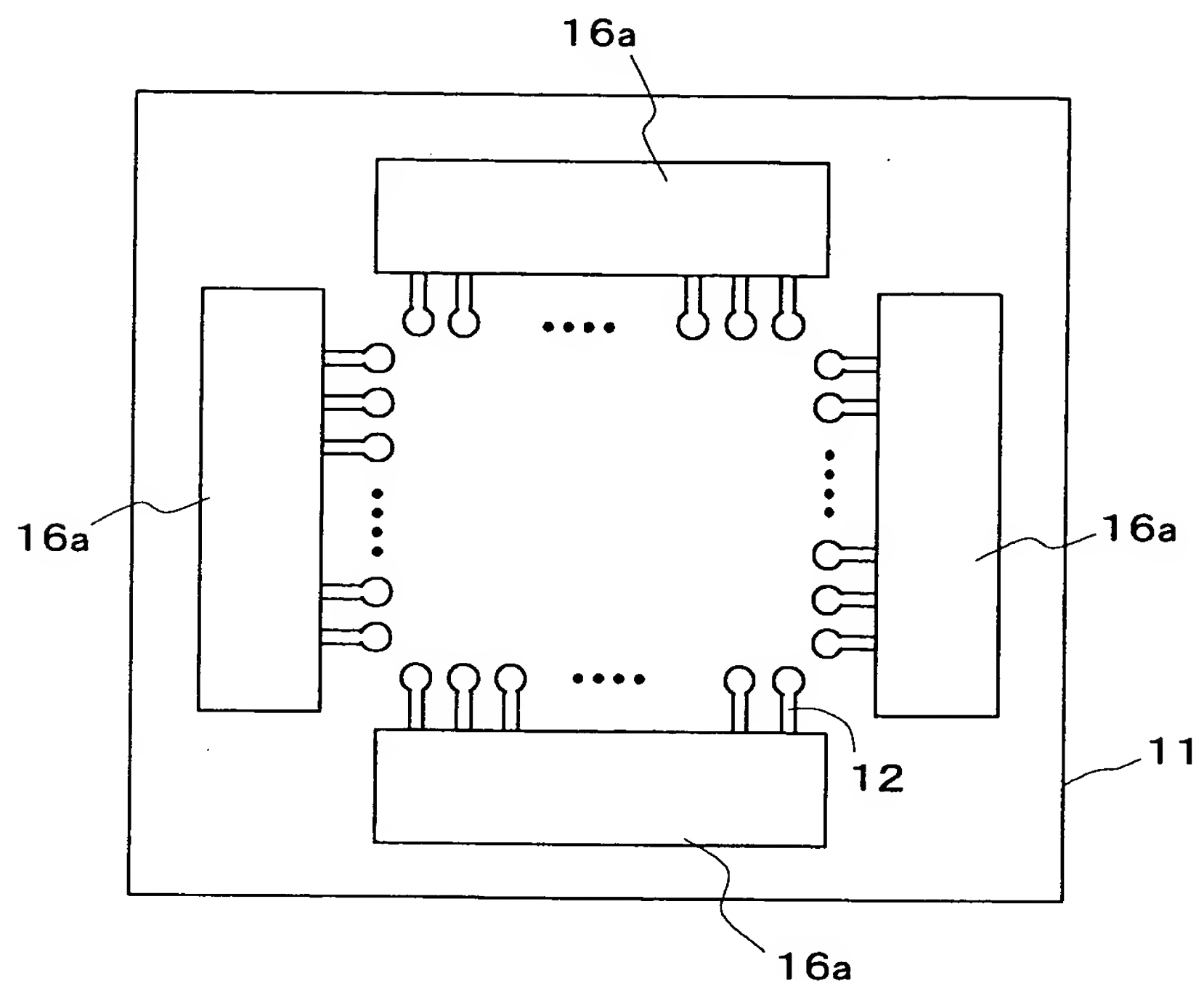


FIG.14B

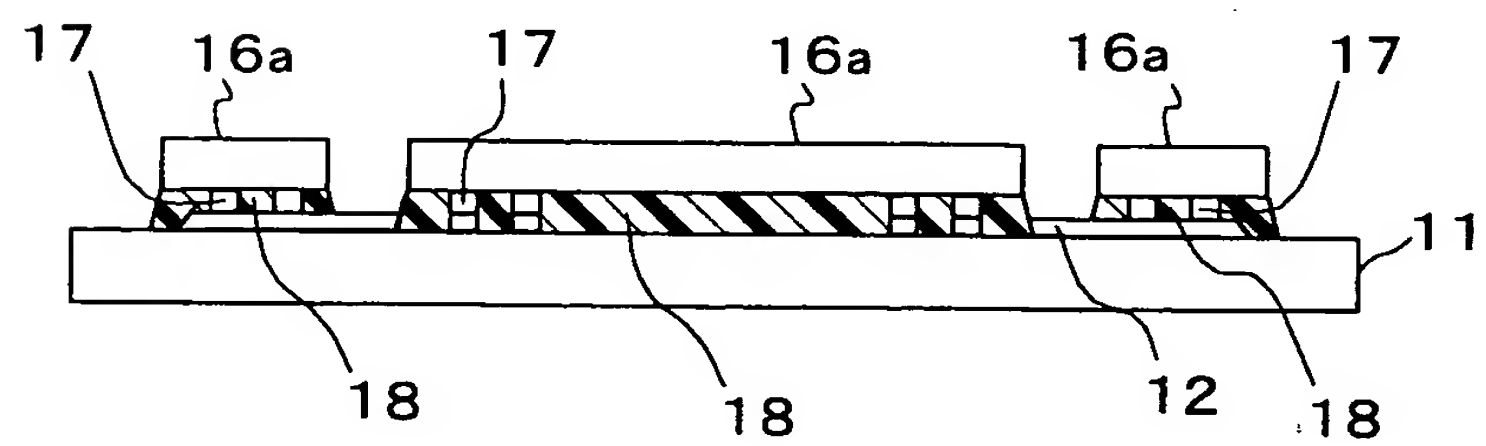


FIG.15A

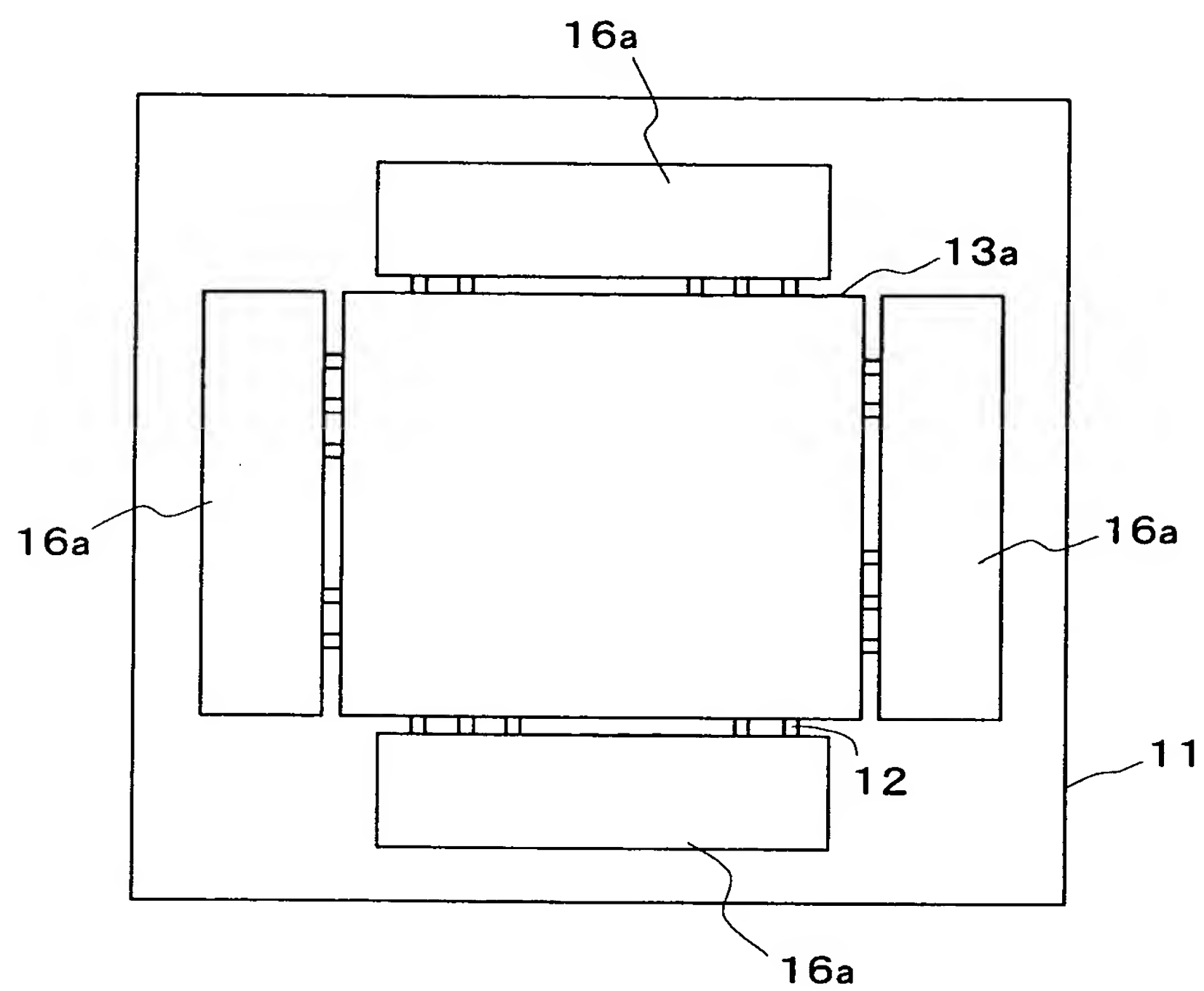


FIG.15B

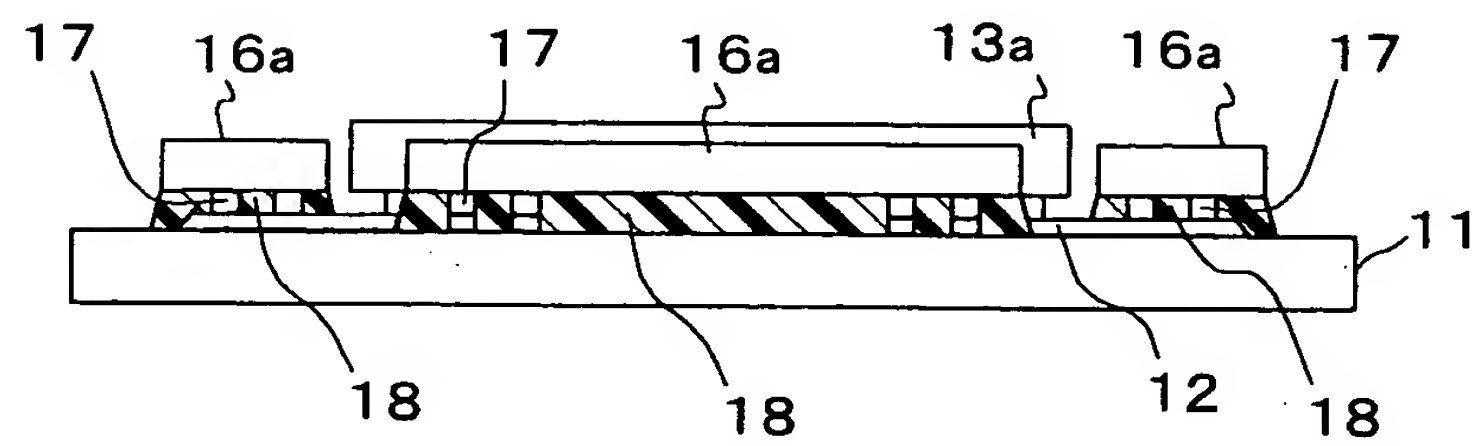




FIG. 16A

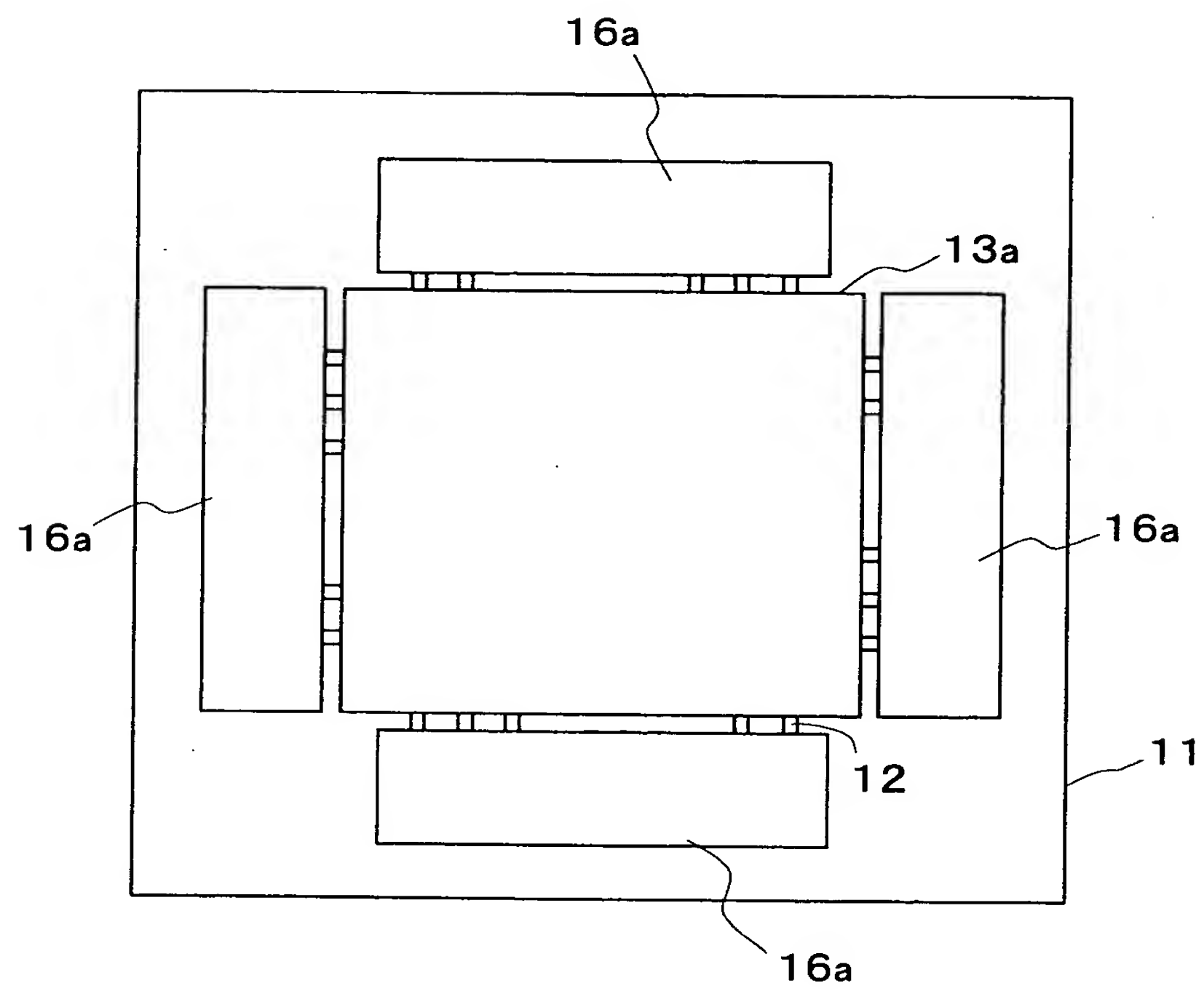


FIG. 16B

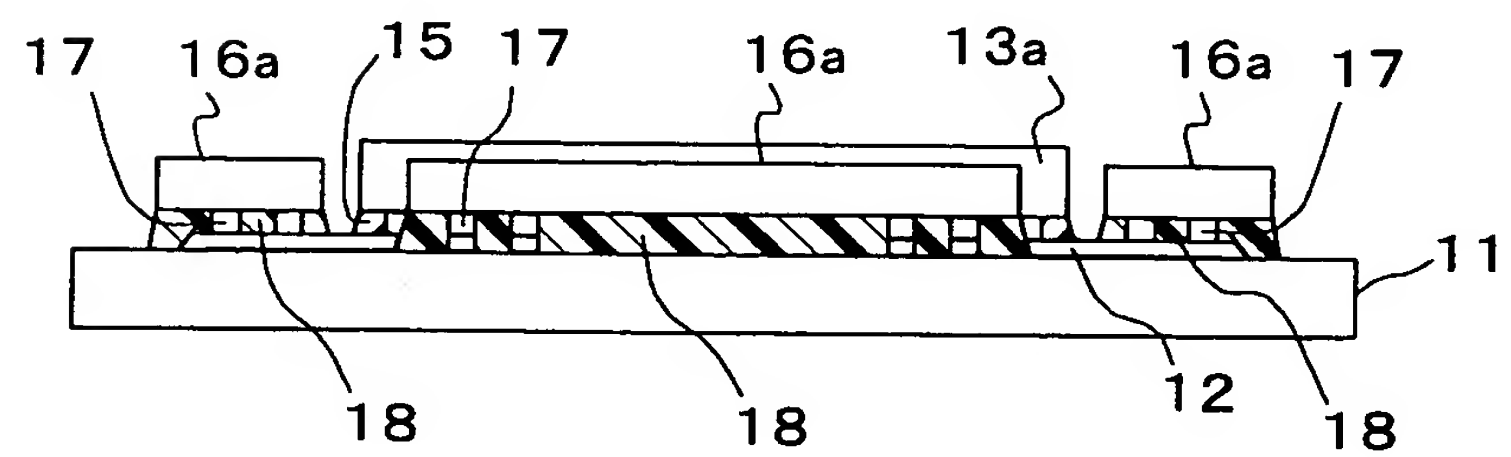


FIG.17

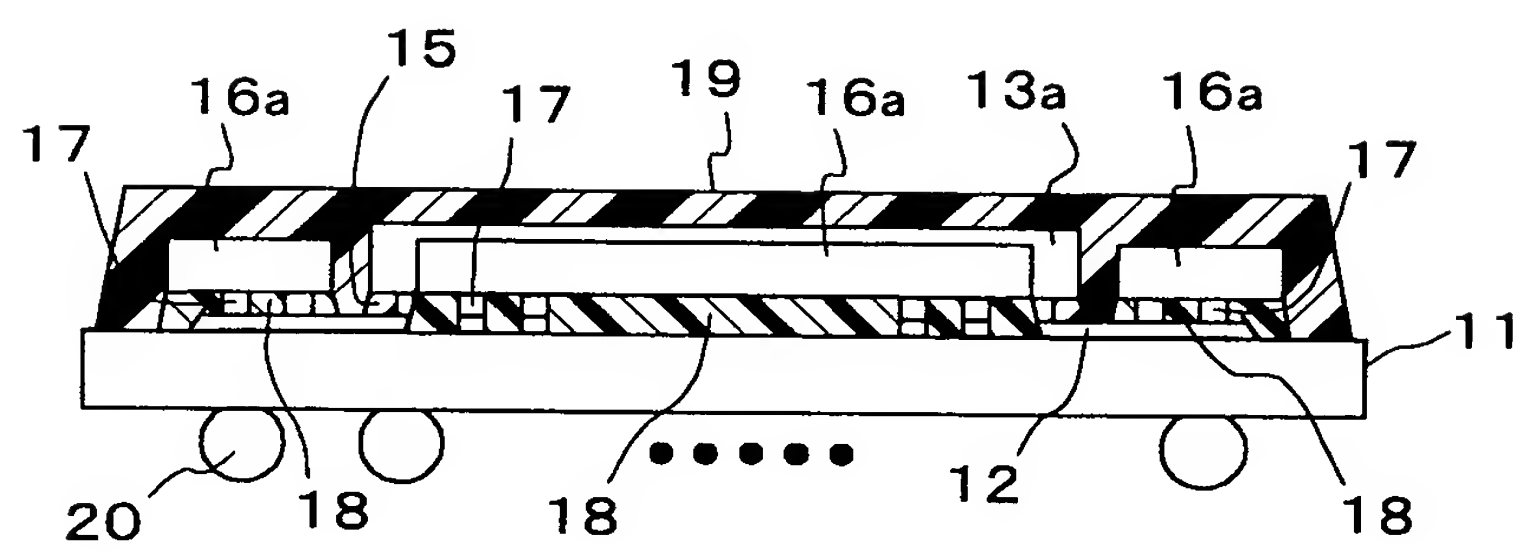


FIG.18A

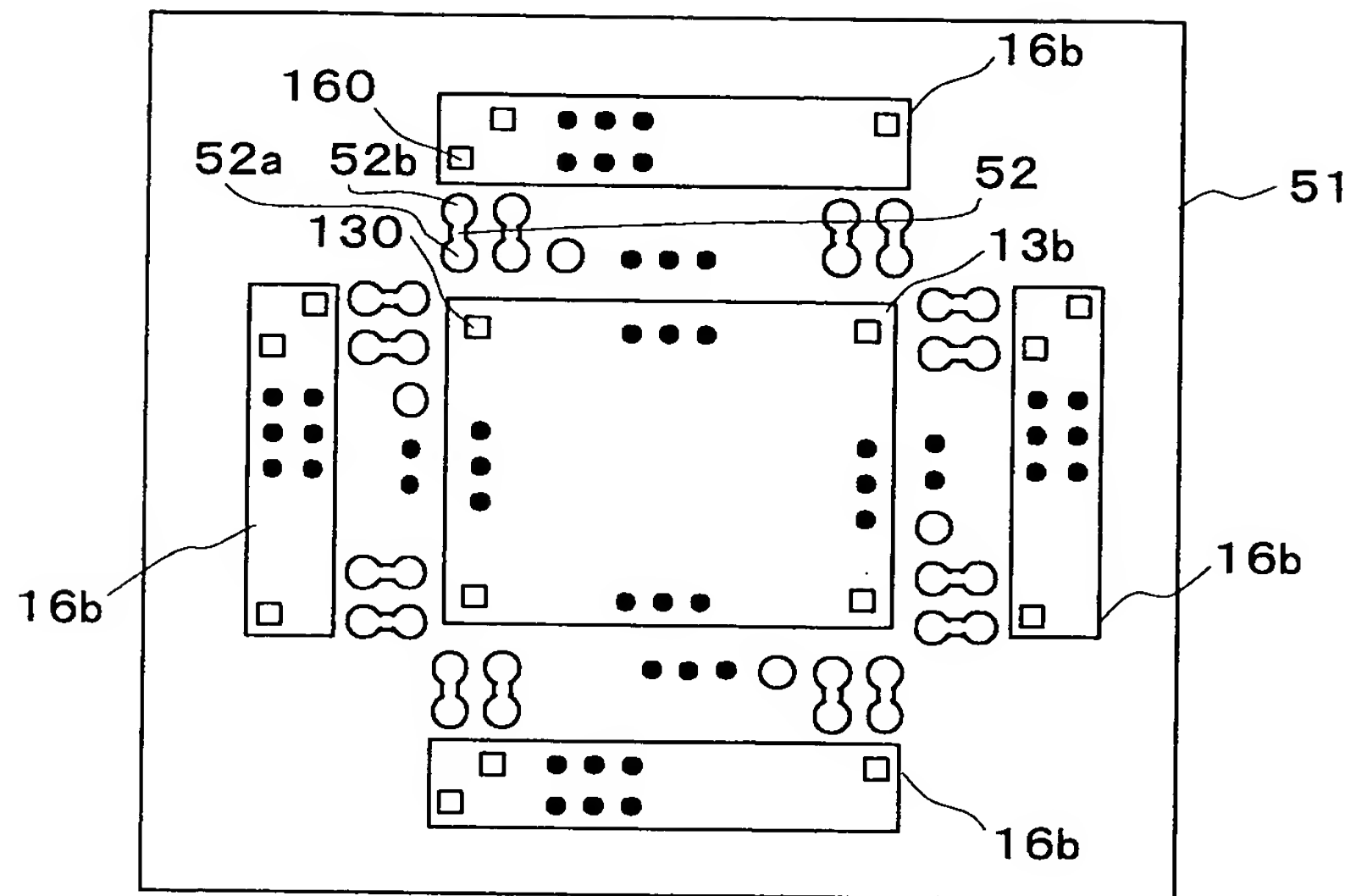


FIG.18B

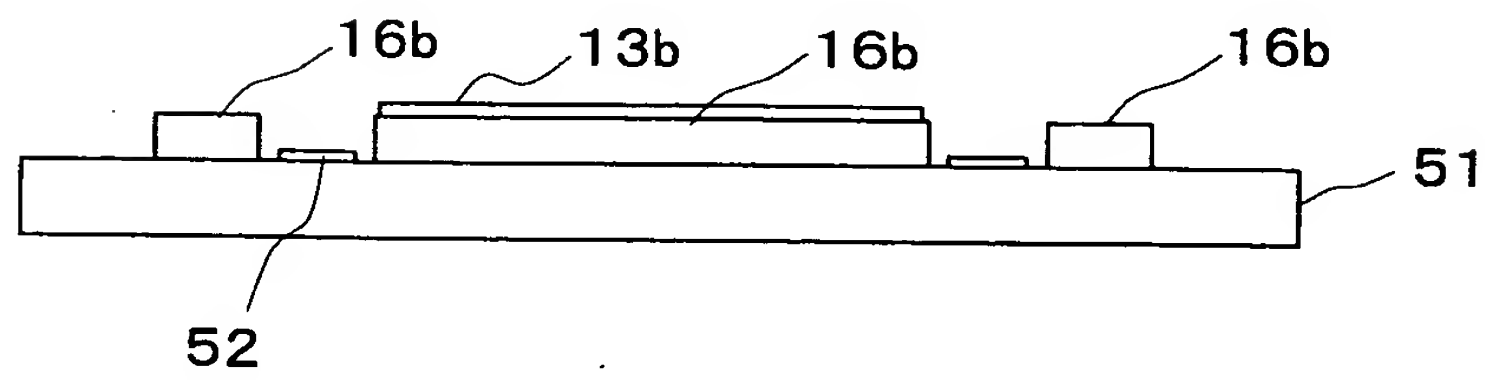


FIG.19A

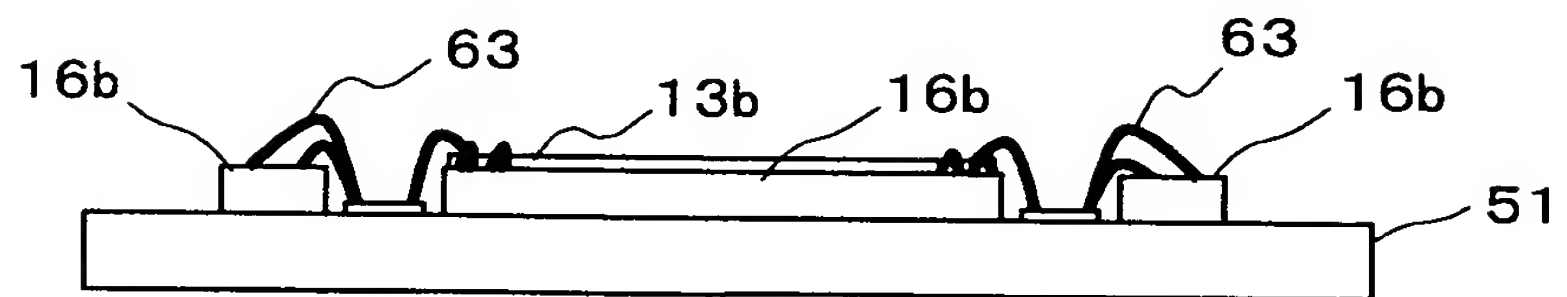


FIG.19B

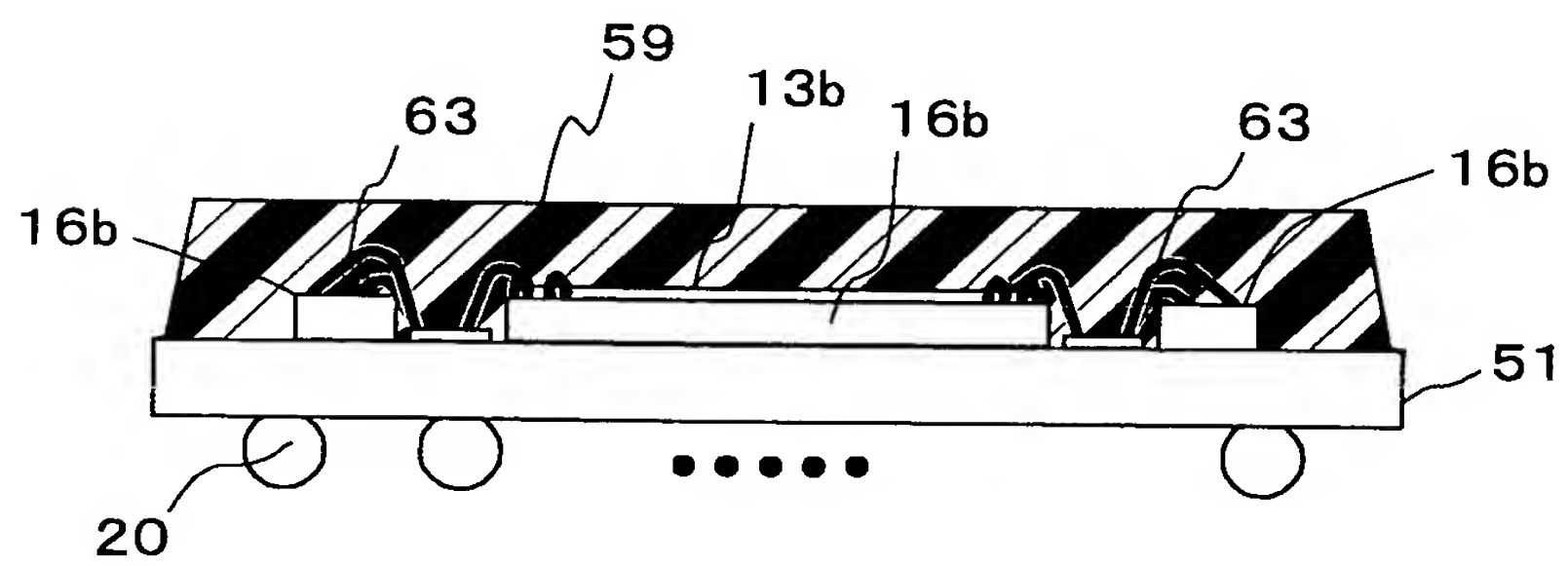


FIG.20A

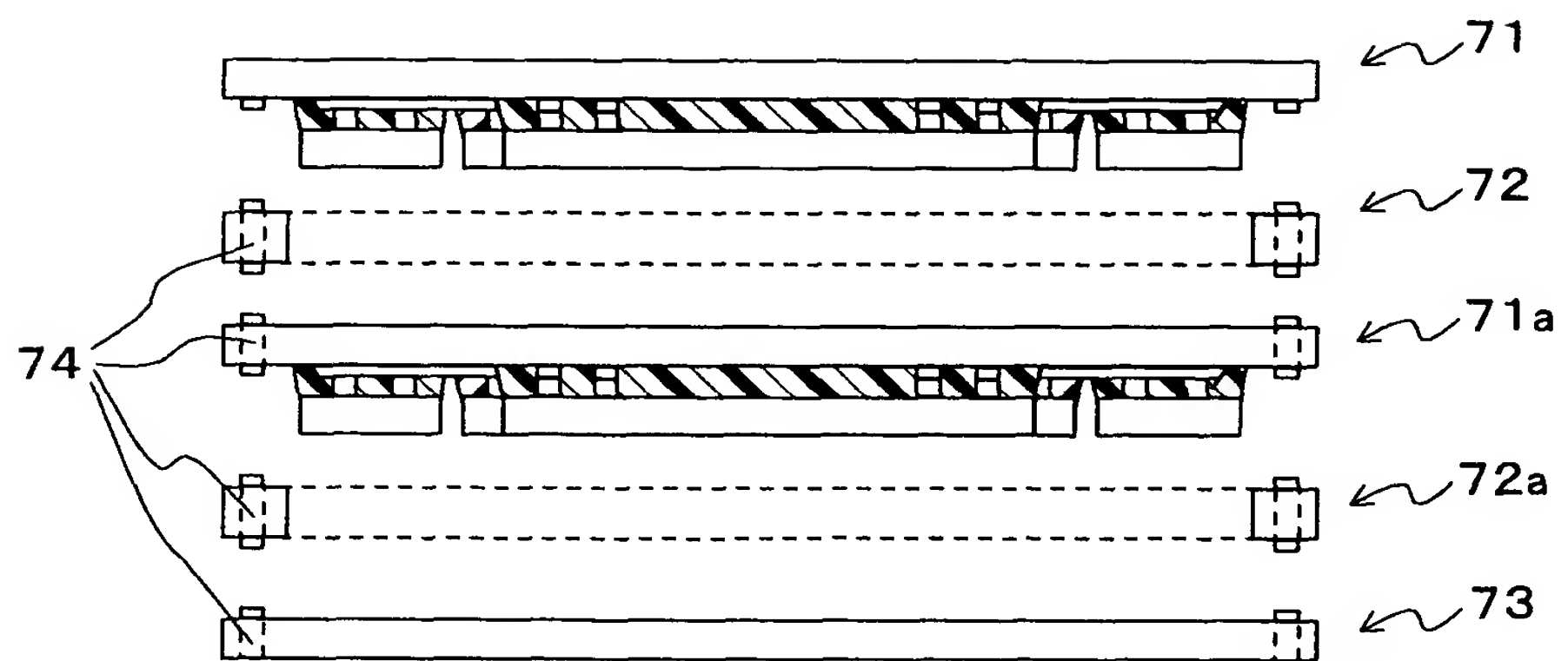
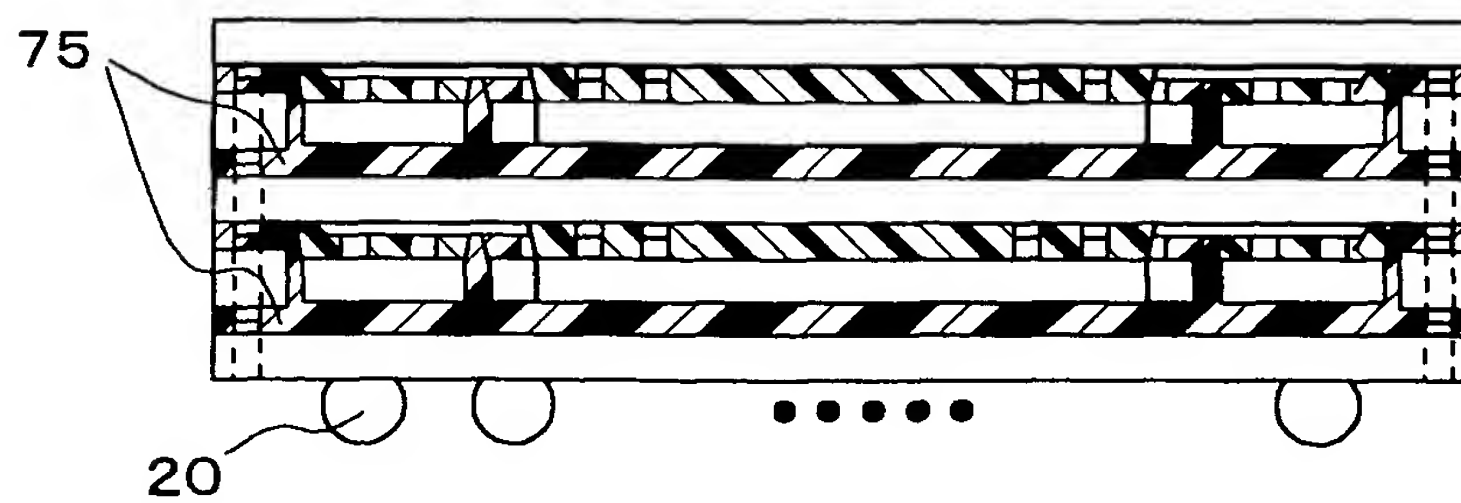
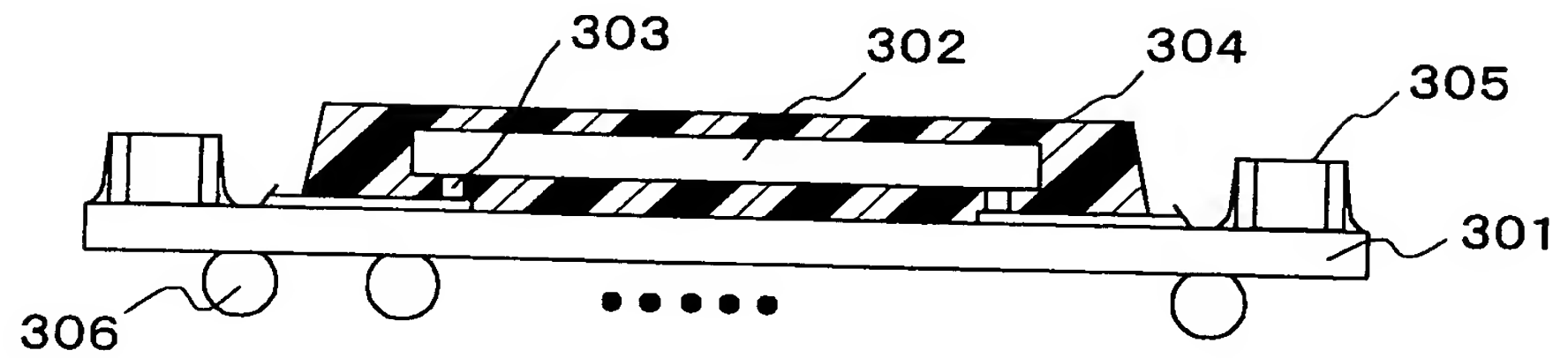


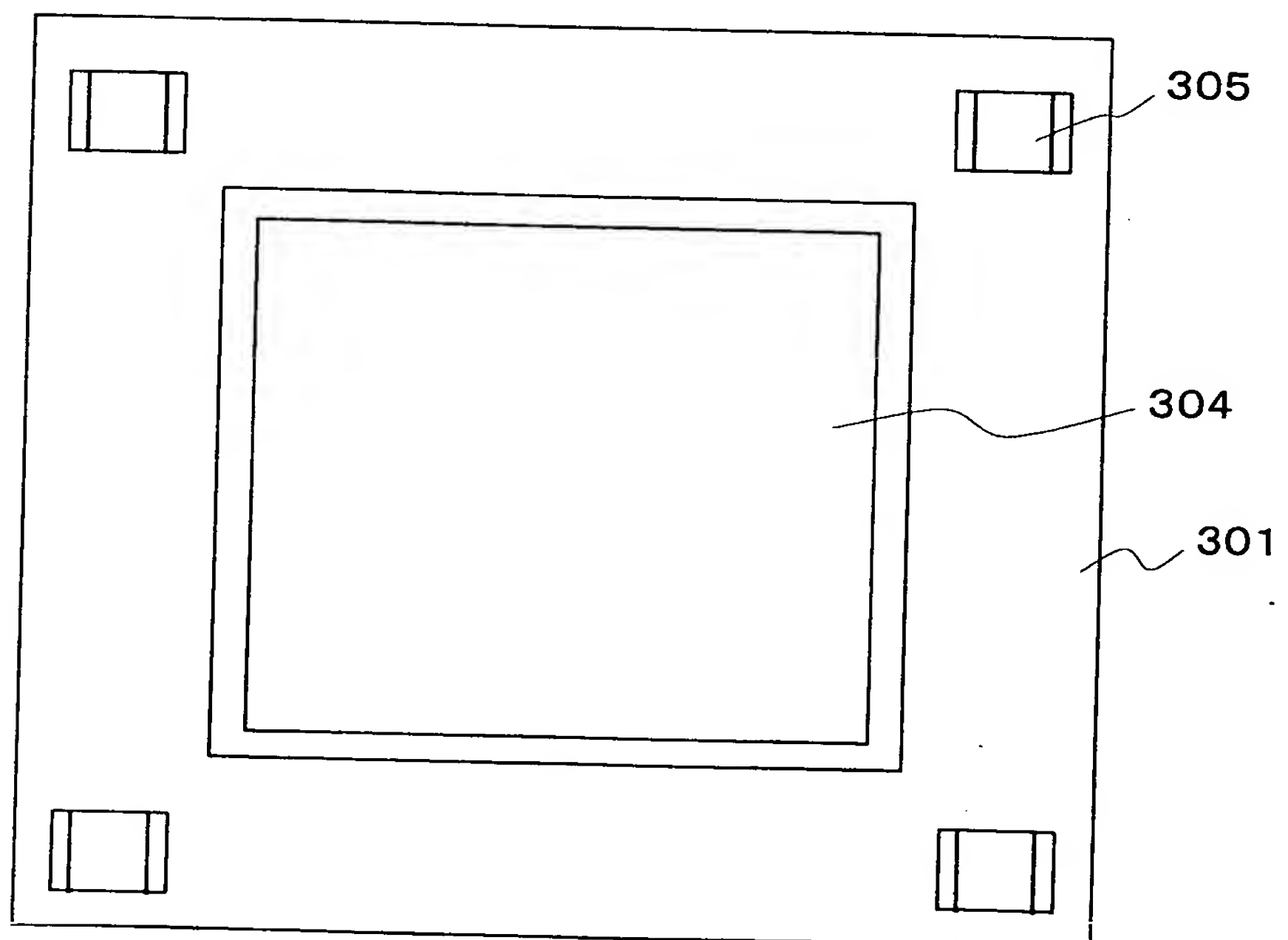
FIG.20B



**FIG.21A**  
PRIOR ART



**FIG.21B**  
PRIOR ART



**FIG.22**  
PRIOR ART

